

FIG. 1

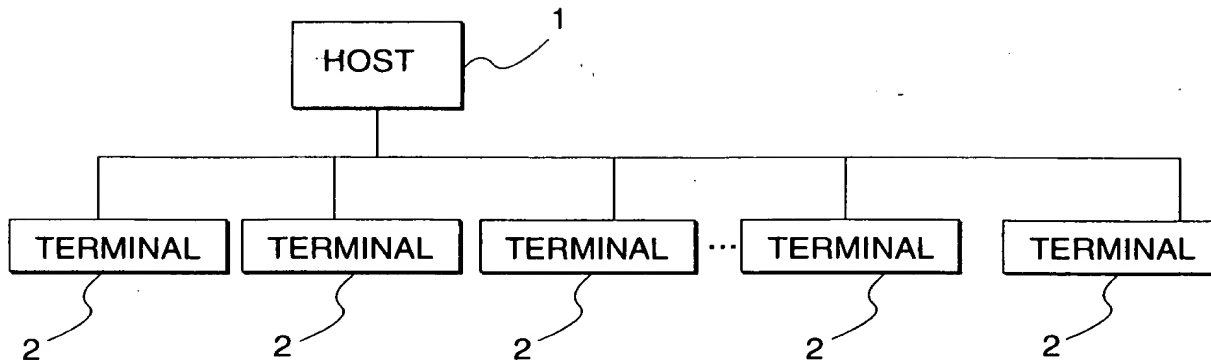


FIG. 2

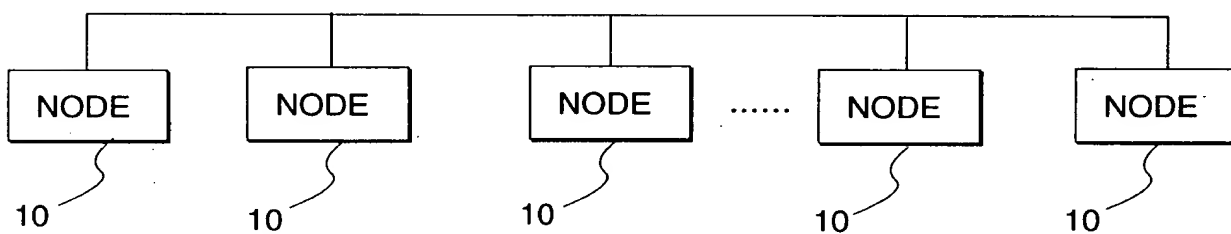


FIG. 3

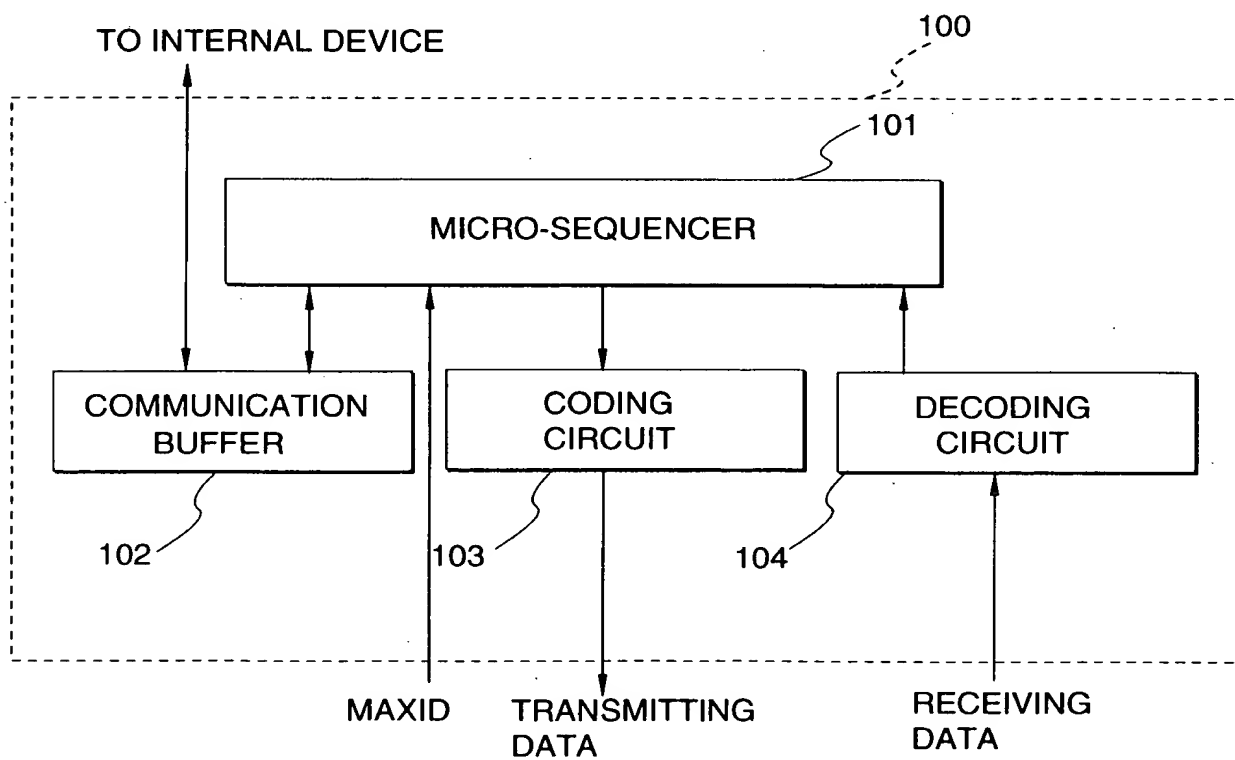


FIG. 4

ALERT	SID	DID	DID	CP	DATA 0	DATA 1		DATA N	CRC	CRC
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FIG. 5

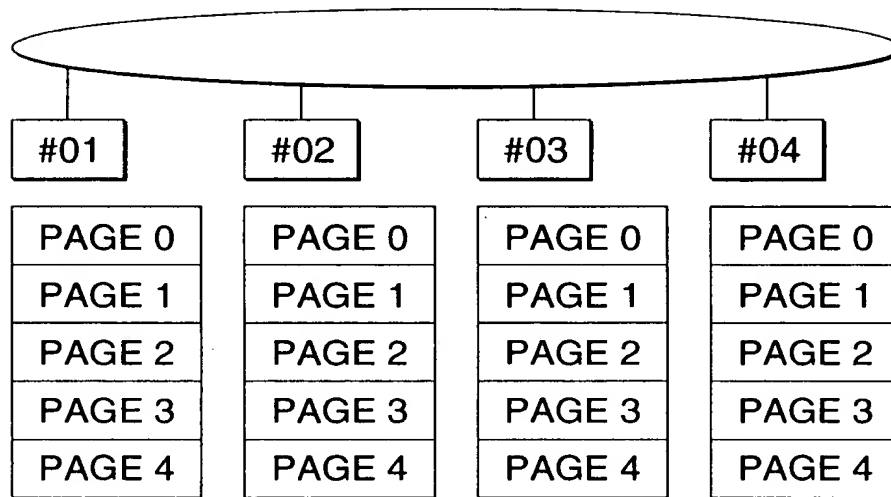


FIG. 6

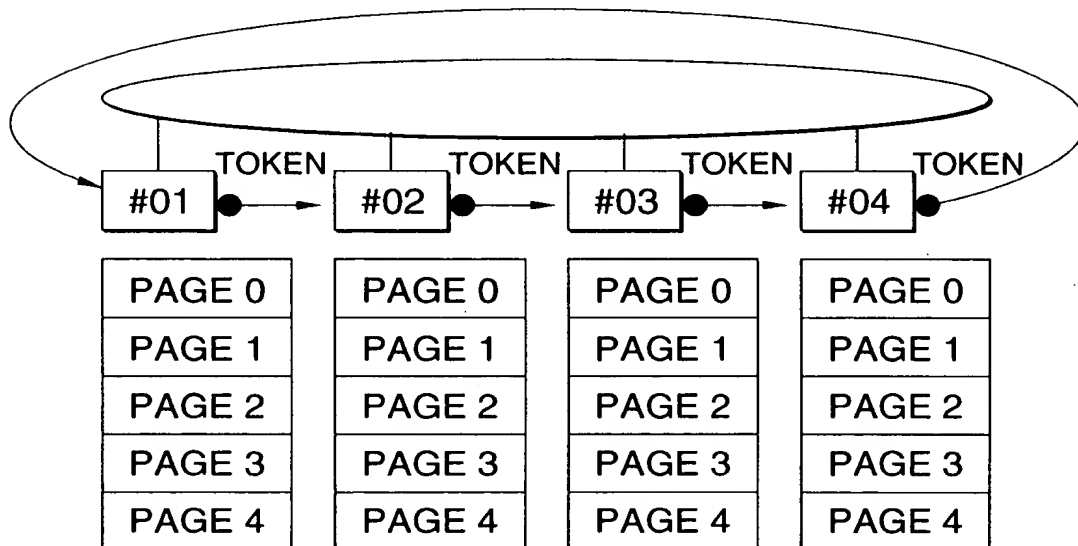


FIG. 7

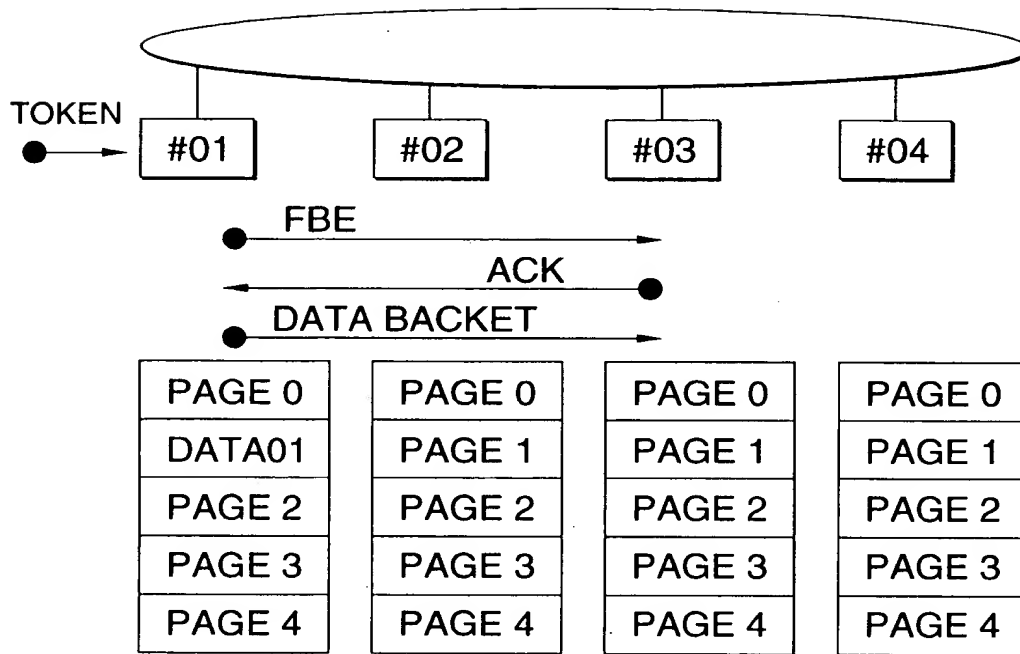


FIG. 8

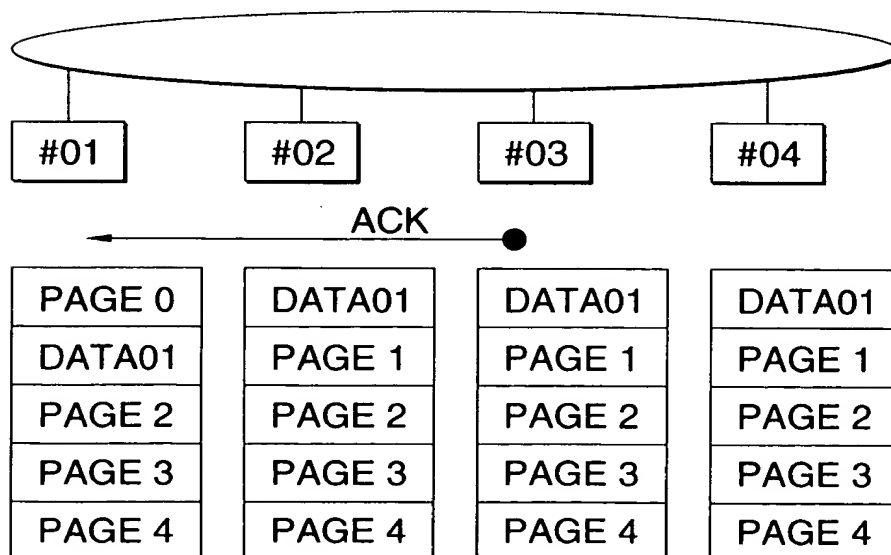


FIG. 9

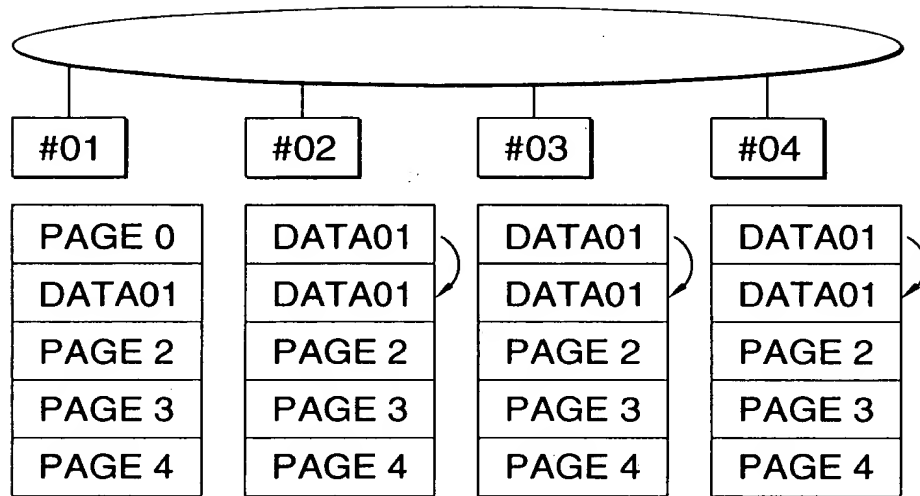


FIG. 10

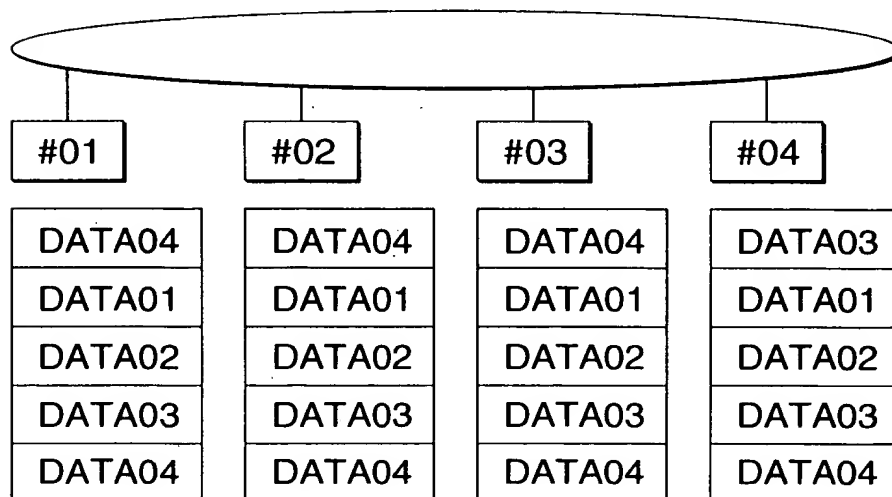


FIG. 11

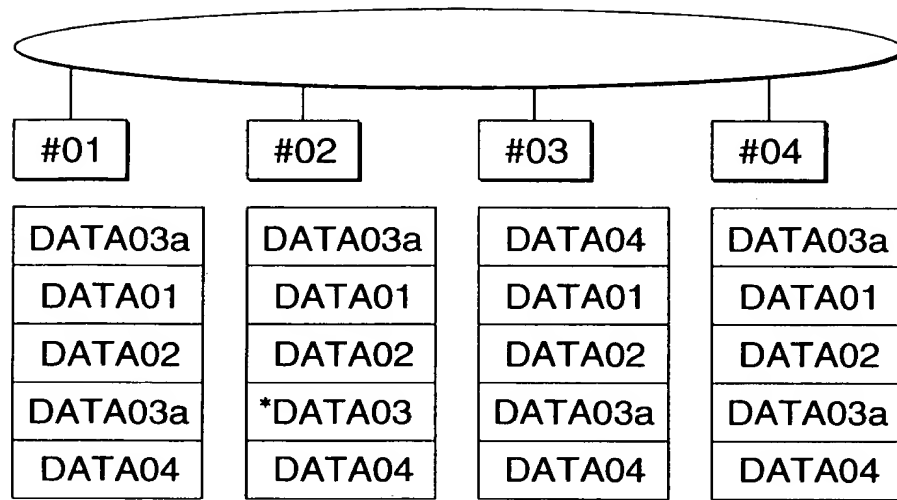


FIG. 12

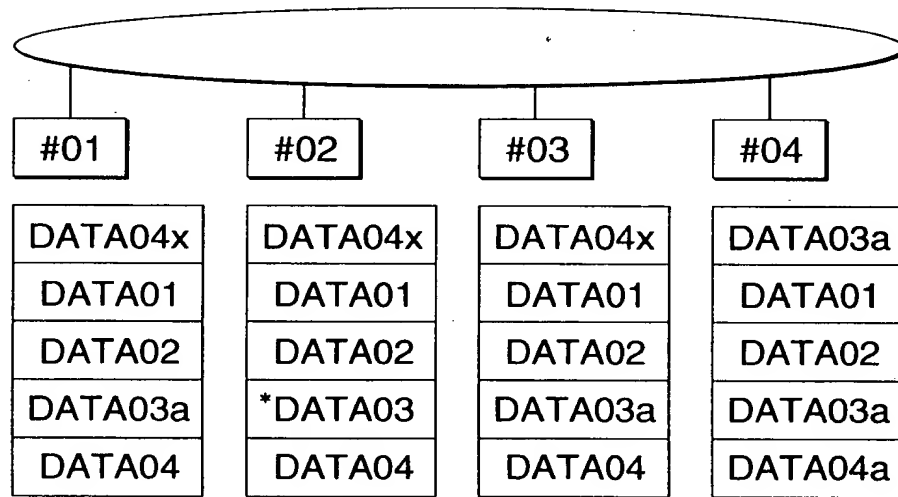


FIG. 13

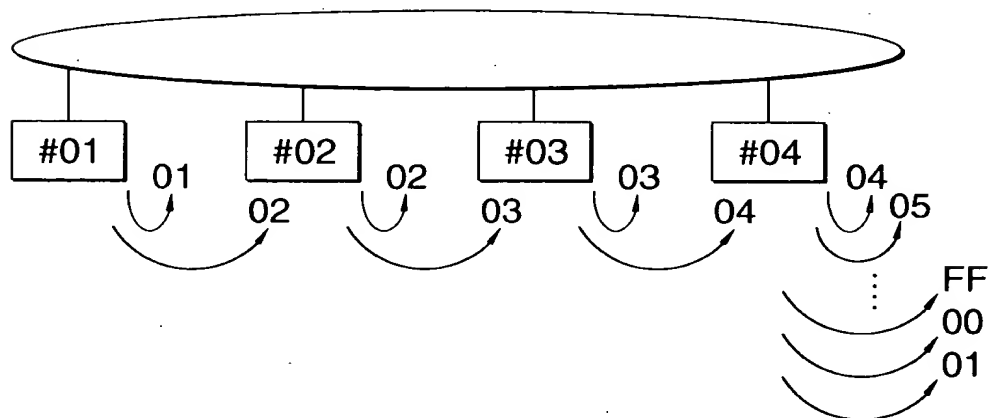


FIG. 14

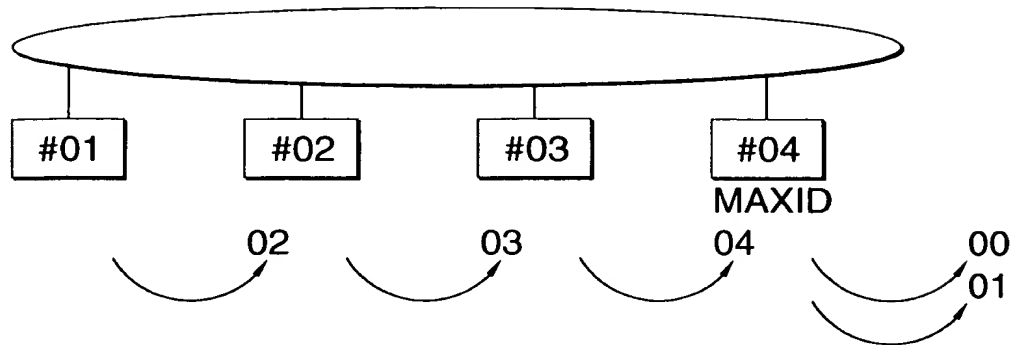


FIG. 15

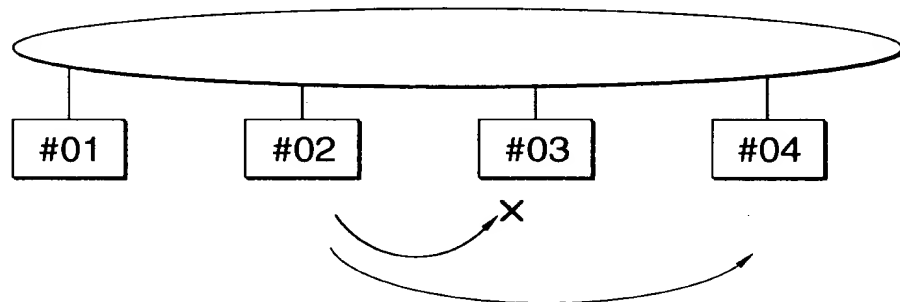


FIG. 16

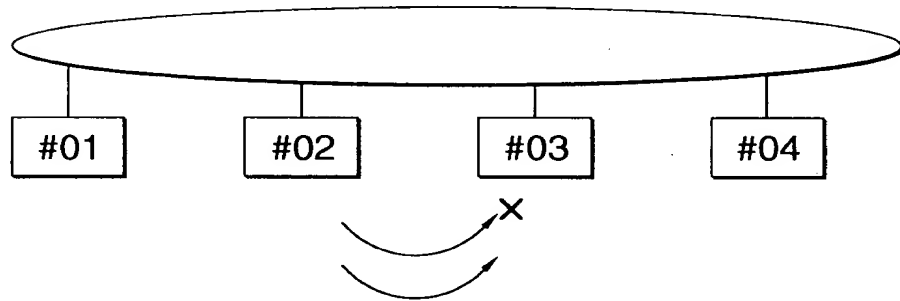
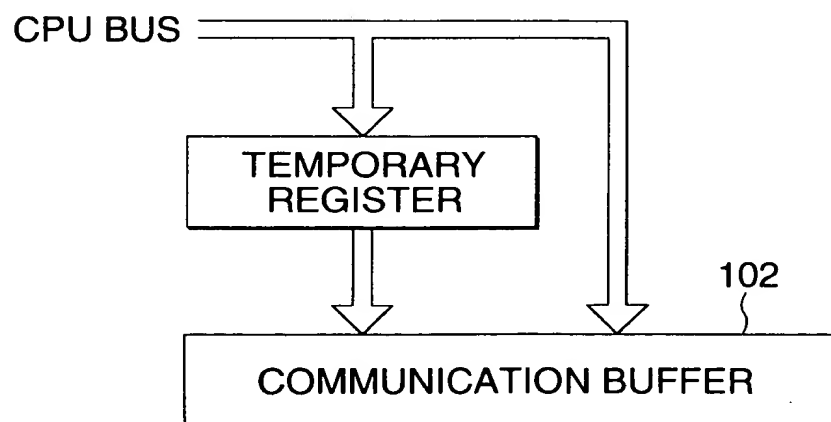


FIG. 17



Timing diagram for the first two write operations:

Phase	Data Bus	Temporary Register	Communication Buffer
BEFORE WRITING	05		05FF
WRITING FIRST BUFFER	06	05	05FF
AFTER WRITING	06	06	05FF
WRITING SECOND BUFFER	00	05FF	0600

FIG. 19

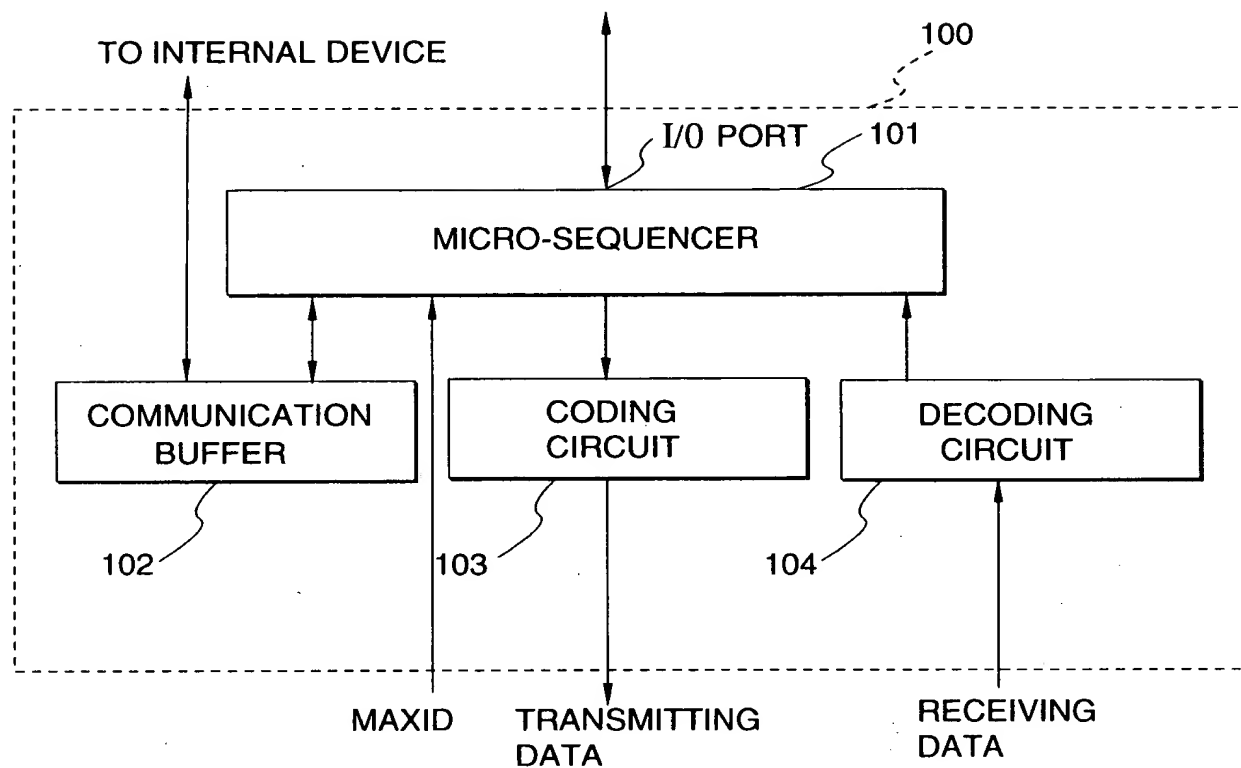


FIG. 20

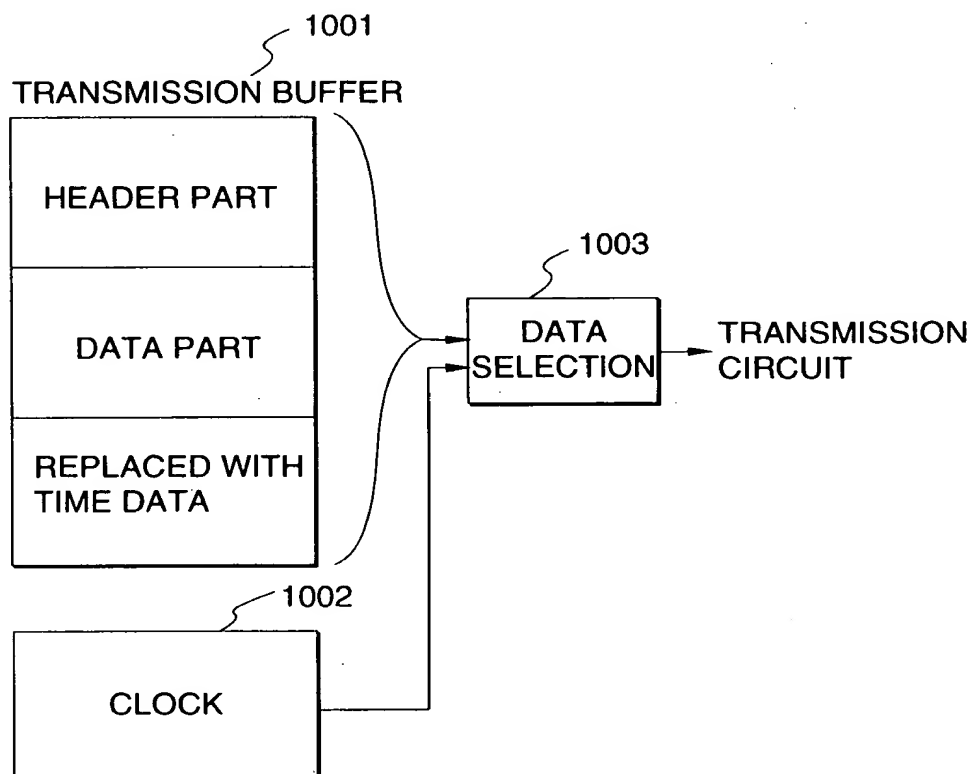


FIG. 21

ALERT	SID	DID	DID	CP	DATA 0		TIME DATA	TIME DATA	CRC	CRC
(DATA N - 1) (DATA N)										

SECRET



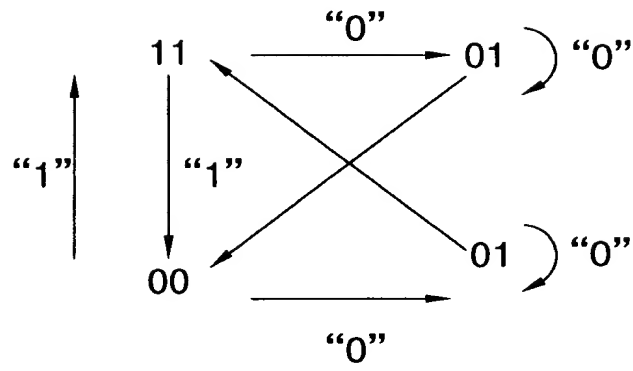
SECRET



SECRET



FIG. 25



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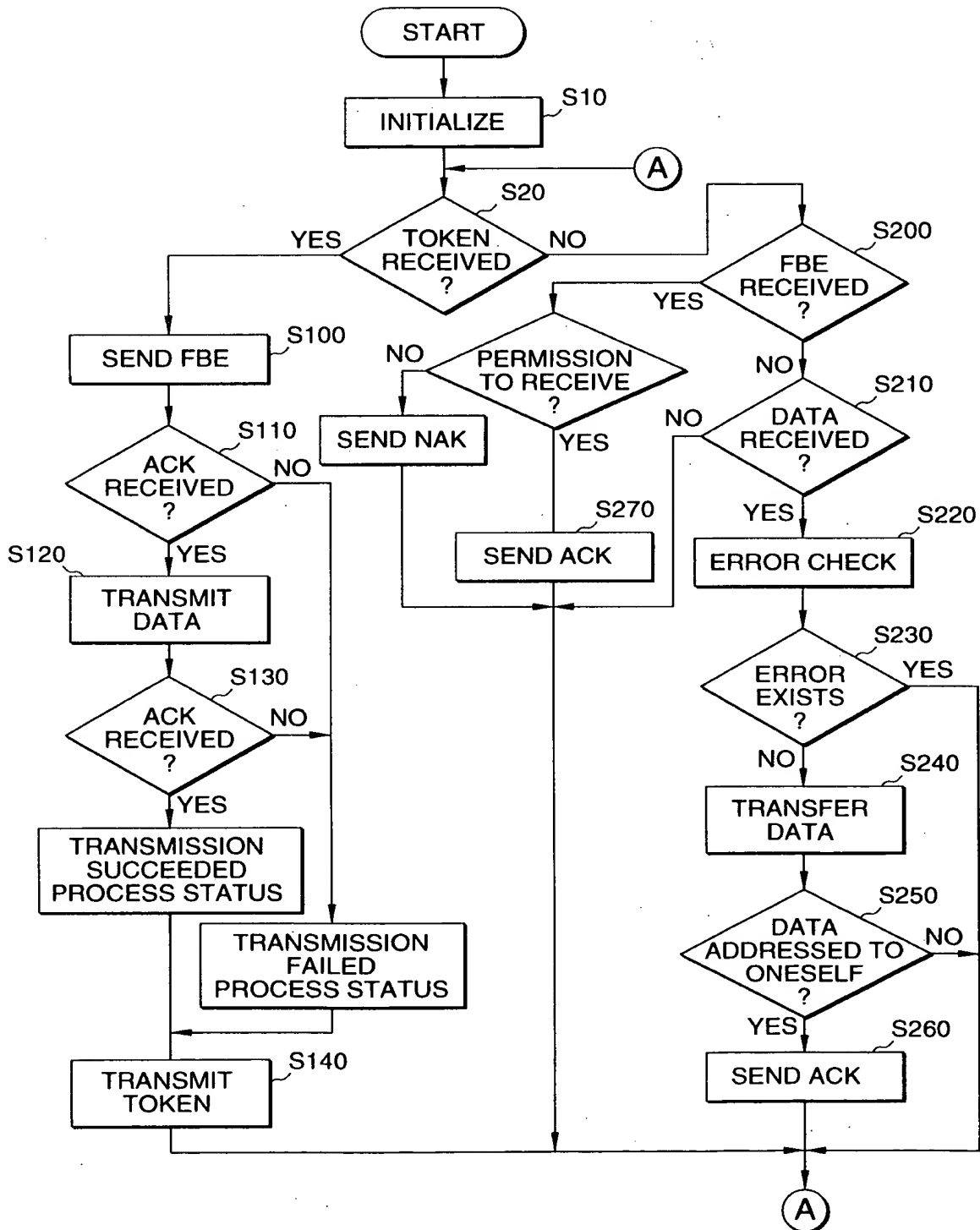


FIG. 27

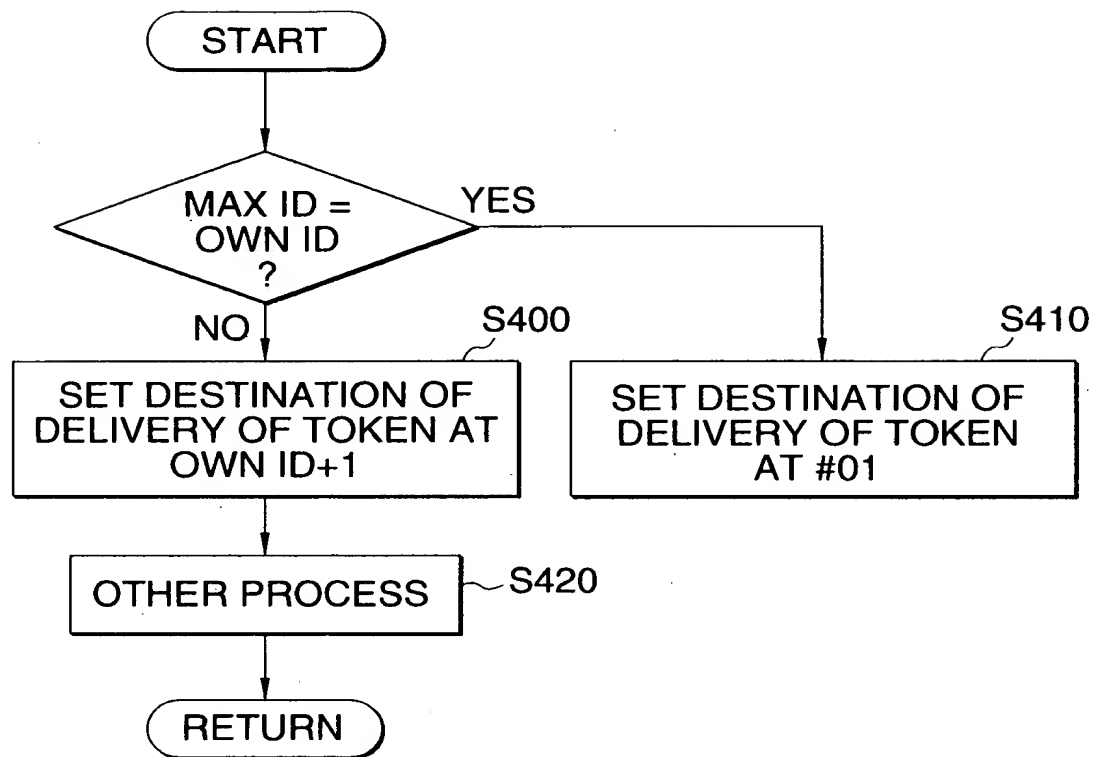


FIG. 28

